What is claimed is:

1. A method for error-correcting data reproduced from a recording medium to which data is recorded according to a data format in which data that is applied with error-correcting coding in a direction different from a recording direction on the recording medium is interleaved and recorded with synchronization signals, the method comprising:

reproducing data from the recording medium, deinterleaving the reproduced data, and storing it to a first memory while arbitrating data input/output to/from the first memory;

determining whether a predetermined amount of data has been stored to the first memory;

permitting transfer of data stored in the first memory to a second memory, based on the result of the determination;

transferring the reproduced data from the first memory to the second memory when the data transfer is permitted while arbitrating input/output to the second memory;

error-correcting the reproduced data stored in the second memory; and

externally outputting from the second memory user data contained in the error-corrected reproduced data.

2. The error-correcting method according to claim 1, wherein the predetermined amount of data is greater than an interleave length.

3. The error-correcting method according to claim 2, wherein the predetermined amount of data is an integer multiple of the interleave length.

4. The error-correcting method according to claim 3, wherein the second memory has a predetermined bus width as the recording and reproducing unit, and the predetermined amount of data is equal to the interleave length multiplied by the predetermined bus width.

5. The error-correcting method according to claim 3, wherein a capacity of the first memory is at least twice the predetermined amount of data.

6. The error-correcting method according to claim 1, wherein the arbitrating input/output to the first memory assigns higher priority to data input to the first memory with data deinterleaved and than data output to the second memory for data transfer.

7. The error-correcting method according to claim 1, wherein a capacity of the first memory is at least three times the predetermined amount of data, and the first memory is implemented with three pages memory management.

8. The error-correcting method according to claim 7, wherein the determining determines that the predetermined amount of data has been stored when, due to loss of synchronization, the predetermined amount of data is not stored to the first memory.

9. An error-correcting circuit for correcting errors in data reproduced from a recording medium to which data is recorded according to a data format in which data that is applied with error-correcting coding in a direction different from a recording direction on the recording medium is interleaved and recorded with synchronization signals, the circuit comprising:

a first memory for temporarily storing data

reproduced from the recording medium according to the data format;

a first arbitration unit that arbitrates data input/output to/from the first memory;

an input controller that stores, while deinterleaving, the reproduced data to the first memory;

an evaluating unit that determines whether a predetermined amount of data has been stored to the first memory;

a second memory;

a second arbitration unit that arbitrates input/output to/from the second memory;

a data transfer permitting unit that permits transfer of the data stored in the first memory to the second memory, based on the result from the evaluating unit;

a data transfer unit that transfers the reproduced data from the first memory to the second memory when data transfer is permitted by the data transfer permitting unit;

an error-correcting unit that error-corrects the reproduced data stored in the second memory; and

an output controller that outputs, from the second memory, user data contained in the reproduced data from which errors have been removed by the error-correcting unit.

10. The error-correcting circuit according to claim 9, wherein the predetermined amount of data is greater than an interleave length.

11. The error-correcting circuit according to claim 10, wherein the predetermined amount of data is an integer multiple of the interleave length.

12. The error-correcting circuit according to claim 12, wherein the second memory has a predetermined bus width as the recording and reproducing unit, and the predetermined amount of data is equal to the interleave length multiplied by the predetermined bus width.

13. The error-correcting circuit according to claim 11, wherein a capacity of the first memory is at least twice the predetermined amount of data.

14. The error-correcting circuit according to claim 9, wherein, during arbitrating the first memory input/output, the first arbitration unit assigns higher priority to input to the first memory by the input controller than data output from the first memory by the data transfer unit.

15. The error-correcting circuit according to claim 9, wherein a capacity of the first memory is at least three times the predetermined amount of data, and the first memory is implemented with three pages memory management.

16. The error-correcting circuit according to claim 15, wherein the evaluating unit determines that the predetermined amount of data has been stored when due to loss of synchronization the predetermined amount of data is not stored to the first memory.

17. An error-correcting coding method for recording data according to a data format in which data that is applied with error-correcting coding in a direction different from a recording direction on the recording medium is interleaved and recorded with synchronization signals, the method comprising:

storing user data to a first memory while arbitrating input/output to/from the first memory;

applying error-correcting coding to user data stored in the first memory;

transferring the data applied with error-correcting coding from the first memory to a second memory while arbitrating input/output to the second memory;

determining whether a predetermined amount of data has been stored to the second memory;

permitting an output of the data stored in the second memory, based on the result of the determination; and

externally outputting, while interleaving, the data from the second memory.

18. The error-correcting coding method according to claim 17, the predetermined amount of data is greater than an interleave length.

19. The error-correcting coding method according to claim 18, wherein the predetermined amount of data is an integer multiple of the interleave length.

20. The error-correcting coding method according to claim 19, wherein the first memory has a predetermined bus width as the storage and reproducing unit, and the predetermined amount of data is equal to the interleave length multiplied by the predetermined bus width.

21. The error-correcting coding method according to claim 18, wherein a capacity of the second memory is at least twice the predetermined amount of data.

22. The error-correcting coding method according to claim 17, wherein the arbitrating input/output to the second memory assigns higher priority to data deinterleaving and data output from the second memory than

input of the data applied with error-correcting coding to the second memory for data transfer.

23. An error-correcting coding circuit for recording data according to a data format in which data that is applied with error-correcting coding in a direction different from a recording direction on the recording medium is interleaved and recorded with synchronization signals, the circuit comprising:

a first memory;

a first arbitration unit that arbitrates data input/output to/from the first memory;

an input controller that stores user data to the first memory;

an error-correcting coding unit that applies error-correcting coding to user data stored in the first memory;

a second memory that temporarily stores the data applied with error-correcting coding by the error-correcting coding unit;

a data transfer unit that transfers the data applied with error-correcting coding from the first memory to the second memory;

a second arbitration unit that arbitrates data input/output to/from the second memory;

a determination unit that determines whether a predetermined amount of data is stored to the second memory;

a transfer permitting unit that permits transfer of data stored in the second memory based on the result from the determination unit;

a data transfer unit that transfers reproduced data from the first memory to the second memory when data transfer is permitted by the transfer permitting unit; and

an output controller that outputs, while

interleaving, the encoded data from the second memory.

24. The error-correcting coding circuit according to claim 23, the predetermined amount of data is greater than an interleave length.

25. The error-correcting coding circuit according to claim 24, wherein the predetermined amount of data is an integer multiple of the interleave length.

26. The error-correcting coding circuit according to claim 25, wherein the first memory has a predetermined bus width as the storage and reproducing unit, and the predetermined amount of data is equal to the interleave length multiplied by the predetermined bus width.

27. The error-correcting coding circuit according to claim 24, wherein a capacity of the second memory is at least twice the predetermined amount of data.

28. The error-correcting coding circuit according to claim 23, wherein the second arbitration unit assigns higher priority to an output from the output controller than an output from the data transfer unit.

29. A data reproducing apparatus comprising:

an optical head that optically reads information from a recording medium;

a reproducing circuit that digitizes information read from the recording medium to generate a reproduction signal;

a demodulator that demodulates signals from the reproducing circuit;

the error-correcting circuit according to claim 9 that error-corrects the demodulated reproduction signal;

and

a signal processing circuit that decompresses the error corrected signal.

30. A data recording and reproducing apparatus comprising:

an optical head that optically records and reproduces information on a recording medium;

a recording and reproducing circuit that generates a reproduction signal by digitizing information read from the recording medium, and generates a control signal from a recording signal for recording to the recording medium;

a modulator/demodulator that demodulates the reproduction signal or modulates the recording signal;

the error-correcting circuit according to claim 9 that error-correcting the reproduction signal demodulated by the modulator/demodulator;

the error-correcting coding circuit according to claim 23 that applies error-correcting coding to the recording signal; and

a signal processing circuit that applies predetermined signal processing operations to the reproduction signal and the recording signal.

31. A method for reproducing data from a recording medium to which data is recorded in a format having a synchronization code, first recording-order arranged data, and second recording-order arranged data alternating in a predetermined cycle,

the first recording-order arranged data acquired by applying a first interleave to first encoded data, the first encoded data provided by applying with error-correcting coding to first data, and

the second recording-order arranged data

acquired by applying a second interleave to second encoded data, the second encoded data provided by applying with error-correcting coding to second data,

the reproducing method comprising:

separating the recorded data read from the recording medium to generate the synchronization code, the first recording-order arranged data, and the second recording-order arranged data;

generating first code word sequence data by applying a first deinterleave to the first recording-order arranged data;

generating second code word sequence data by applying a second deinterleave to the second recording-order arranged data;

error-correcting the second code word sequence data to generate data error location information corresponding to the order of the second code word sequence data;

applying a second interleave to the data error location information to generate data error location information corresponding to the order of the second recording-order arranged data;

extracting synchronization error information from the synchronization code;

combining, in the recording sequence of the recorded data, the data error location information in the order of the second recording-order arranged data and the synchronization error information to generate first data error location information;

generating erasure pointers from the first data error location information, the erasure pointers indicating positions at which the first data erase and corresponding to the order of the first recording-order arranged data;

applying a first deinterleave to the erasure pointers to generate erasure pointers corresponding to the

order of the first code word sequence data; and

applying error-correcting for erasure to the first code word sequence data, using the erasure pointers corresponding to the order of the first code word sequence data.

32. The data reproducing method according to claim 31, wherein the generating erasure pointers corresponding to the order of the first recording-order arranged data generates erasure pointers by determining from the first data error location information whether errors occur in the second recording-order arranged data or synchronization code continuously in the recording direction of the recorded data.

33. A method for reproducing data from a recording medium to which data is recorded in a format having a synchronization code, first recording-order arranged data, and second recording-order arranged data alternating in a predetermined cycle,

the first recording-order arranged data acquired by applying a first interleave to first encoded data, the first encoded data provided by applying with error-correcting coding to first data, and

the second recording-order arranged data acquired by applying a second interleave to second encoded data, the second encoded data provided by applying with error-correcting coding to second data,

the method comprising:

separating recorded data read from the recording medium to generate the synchronization code, first recording-order arranged data, and second recording-order arranged data,

extracting synchronization error information from the synchronization code,

applying a first deinterleave to the first recording-order arranged data and generating first code word sequence data corresponding to the first recording-order arranged data, and

applying a second deinterleave to the second recording-order arranged data and generating second code word sequence data;

error-correcting the second code word sequence data and generating data error location information corresponding to the order of the second code word sequence data;

generating erasure pointers corresponding to the order of the first recording-order arranged data from the data error location information and synchronization error information, the erasure pointers denoting data erasure locations in the first data; and

applying error-correcting for erasure to the first code word sequence data, using the erasure pointers while applying a first deinterleave to the erasure pointers.

34. A method for reproducing data from a recording medium to which data is recorded in a format having a synchronization code, first recording-order arranged data, and second recording-order arranged data alternating in a predetermined cycle,

the first recording-order arranged data acquired by applying a first interleave to first encoded data, the first encoded data provided by applying with error-correcting coding to first data, and

the second recording-order arranged data acquired by applying a second interleave to second encoded data, the second encoded data provided by applying with error-correcting coding to second data,

the method comprising:

separating the data read from the recording

medium, to generate the synchronization code, the first recording-order arranged data, and the second recording sequence, extracting synchronization error information from the synchronization code and writing to a first memory, applying a first deinterleave to the first recording-order arranged data, generating first code word sequence data, and writing to a second memory, and applying a second deinterleave to the second recording-order arranged data, generating second code word sequence data, and writing to a third memory;

error-correcting the second code word sequence data and writing data error location information corresponding to the order of the second code word sequence data to a fourth memory;

generating erasure pointers denoting erasure locations in the first data and corresponding to the order of the first recording-order arranged data from the data error location information and synchronization error information, and writing to fifth memory; and

applying error-correcting for erasure to the first code word sequence data, using the erasure pointers, while applying, a first deinterleave to the erasure pointers.

35. The data reproducing method according to claim 34, wherein the second memory and third memory are areas in a same buffer memory, and the first code word sequence data and second code word sequence data are written to respectively allocated areas in the buffer memory.

36. The data reproducing method according to claim 35, wherein flags corresponding to the synchronization detection information, first recording-order arranged data, and second recording-order arranged data are set in the order of the recorded data, and a destination of writing is

switched based on these flags between the first memory, a area in the buffer memory for the first code word sequence data, and a area in the buffer memory for the second code word sequence data.

37. The data reproducing method according to claim 34, wherein the second code word sequence data error location information allocates one bit to one byte of the second code word sequence data, and manages error location information for one column of the second code word sequence data using m-bytes (where m is an integer) of data.

38. The data reproducing method according to claim 34, wherein according to a format of the synchronization error information, one byte is allocated to one synchronization error information, and plural bytes of synchronization error information are arranged in the order of the recorded data.

39. The data reproducing method according to claim 34, wherein the first recording-order arranged erasure pointer contains plural bytes, each byte denotes erasure location information, and the bytes are arranged in the order of the first recording-order arranged data.

40. The data reproducing method according to claim 34, wherein the first memory, the fourth memory, and the fifth memory are areas allocated in one small capacity memory.

41. The data reproducing method according to claim 40, wherein the small capacity memory has two areas for storing the synchronization error information, one area for storing the data error location information, and one area for storing the erasure pointers.

42. A method for reproducing data from a recording medium to which data is recorded in a format having a synchronization code, first recording-order arranged data, and second recording-order arranged data alternating in a regular cycle,

the first recording-order arranged data acquired by applying a first interleave to first encoded data, the first encoded data provided by applying with error-correcting coding to first data, and

the second recording-order arranged data acquired by applying a second interleave to second encoded data, the second encoded data provided by applying with error-correcting coding to second data,

the reproducing method comprising:

separating data from the recorded data read from the recording medium to generate the synchronization code, the first recording-order arranged data, and the second recording-order arranged data;

dividing the first recording-order arranged data into plural data segments, applying a first deinterleave to each data segment, and generating plural first code word sequence data segments;

assembling the plural first code word sequence data segments to generate the first code word sequence data;

applying a second deinterleave to the second recording-order arranged data to generate the second code word sequence data;

error-correcting the second code word sequence data and generating data error location information corresponding to the order of the second code word sequence data;

applying the second deinterleave to the data error location information and generating data error location information corresponding to the order of the

second recording-order arranged data;

extracting synchronization error information from the synchronization code;

generating first data error location information denoting locations in which errors occur in the first data, by combining, in the recording sequence, the synchronization error information and the data error location information in the order of the second recording-order arranged data;

generating first recording-order arranged erasure pointers which indicate erasure locations in the first data and correspond to the order of the first recording-order arranged data, from the first data error location information;

applying a first deinterleave to the erasure pointers to generate erasure pointers corresponding to the order of the first code word sequence data; and

applying error-correcting for erasure to the first code word sequence data, using the erasure pointers in the order of the first code word sequence data.

43. The data reproducing method according to claim 42, wherein the generating erasure pointers in the order of the first recording-order arranged data determines from the first data error location information whether the second recording-order arranged data errors or synchronization code errors occur continuously in the recording direction of the recorded data to generate erasure pointers.

44. A method for reproducing data from a recording medium to which data is recorded in a format having a synchronization code, first recording-order arranged data, and second recording-order arranged data alternating in a regular cycle,

the first recording-order arranged data acquired

by applying a first interleave to first encoded data, the first encoded data provided by applying error-correcting coding to first data, and

the second recording-order arranged data acquired by applying a second interleave to second encoded data, the second encoded data provided by applying error-correcting to second data,

the reproducing method comprising:

separating data read from the recording medium, to generate the synchronization code the first recording-order arranged data, and the second recording-order arranged data, extracting synchronization error information from the synchronization code, dividing the first recording-order arranged data into plural data segments, applying a first deinterleave to each data segment to generate plural first code word sequence data segments, and applying a second deinterleave to the second recording-order arranged data to generate second code word sequence data;

assembling the plural first code word sequence data segments to generate first code word sequence data;

error-correcting the second code word sequence data to generate data error location information corresponding to the order of the second code word sequence data;

generating erasure pointers denoting erasure locations in the first data in the order of the first recording-order arranged data from the data error location information and synchronization error information; and

applying error-correcting for erasure to the first code word sequence data using the erasure pointers while deinterleaving the erasure pointers with a first deinterleaving.

45. A method for reproducing data from a recording

medium to which data is recorded in a format having a synchronization code, first recording-order arranged data, and second recording-order arranged data alternating in a predetermined cycle,

the first recording-order arranged data acquired by applying a first interleave to first encoded data, the first encoded data provided by applying error-correcting coding to first data, and

the second recording-order arranged data acquired by applying a second interleave to second encoded data, the second encoded data provided by applying error-correcting coding to second data,

the reproducing method comprising:

separating recorded data read from the recording medium to generate the synchronization code, the first recording-order arranged data, and the second recording-order arranged data,

extracting synchronization error information from the synchronization code to write to a first memory, dividing the first recording-order arranged data into plural data segments, applying a first deinterleave to each data segment to generate plural first code word sequence data segments and writing them to a second memory, and applying a second deinterleave to the second recording-order arranged data to generate second code word sequence data and writing them to a third memory;

sequentially writing the first code word sequence data segments from the second memory to a fourth memory to generate first code word sequence data;

error-correcting the second code word sequence data and writing data error location information corresponding to the order of the second code word sequence data to a fifth memory;

generating erasure pointers denoting errors in the first data from the data error location information and

synchronization error information, and writing the erasure pointers to a sixth memory, the erasure pointers arranged in the order corresponding to the order of the first recording-order arranged data; and

applying error-correcting for erasure to the first code word sequence data using the erasure pointers while applying a first deinterleave to the erasure pointers.

46. The data reproducing method according to claim 45, wherein the capacity of the second memory is smaller than the size of the first recording-order arranged data.

47. The data reproducing method according to claim 45, wherein the third memory and fourth memory are areas in the same buffer memory, and the first code word sequence data and second code word sequence data are written to respectively allocated areas in the buffer memory.

48. The data reproducing method according to claim 45, wherein flags corresponding to the synchronization detection information, the first recording-order arranged data, and the second recording-order arranged data are set in the order of the recorded data, and a destination of writing is switched based on these flags between the first memory, the second memory, and an area in the buffer memory for the second code word sequence data.

49. The data reproducing method according to claim 45, wherein the data error location information in the order of the second code word sequence data allocates one bit to one byte of the second code word sequence data, and manages error location information for one column of second code word sequence data using m-bytes (where m is an integer) of data.

50. The data reproducing method according to claim 45, wherein according to a format of the synchronization error information, one byte is allocated to one synchronization detection information, and plural bytes of synchronization detection information are arranged in the order of the recorded data.

51. The data reproducing method according to claim 45, wherein the first recording-order arranged erasure pointer contains plural bytes, each byte denotes erasure location information, and the bytes are arranged in the order of the first recording-order arranged data.

52. The data reproducing method according to claim 45, wherein the first memory, the fifth memory, and the sixth memory are areas allocated in one small capacity memory.

53. The data reproducing method according to claim 52, wherein the small capacity memory has two areas for storing the synchronization error information, one area for storing the second data error location information, and one area for storing the first recording-order arranged erasure pointers.

54. A method for recording data to a recording medium according to a format having alternating first data and second data, comprising:

error-correcting the first data to generate first code word sequence data;

error-correcting the second data to generate second code word sequence data;

generating synchronization codes;

applying a first interleave to the first code word sequence data to generate first recording-order arranged data;

applying a second interleave to the second code word sequence data to generate second recording-order arranged data; and

arranging alternately the synchronization codes, the first recording-order arranged data, and the second recording-order arranged data in a predetermined cycle to record them to the recording medium.

55. A method for recording data to a recording medium according to a format having alternating first data and second data, comprising:

error-correcting the first data and writing first code word sequence data to a first memory;

error-correcting the second data and writing second code word sequence data to a second memory;

generating synchronization codes; and

reading the first code word sequence data written in the first memory while applying a first interleave to the first code word sequence data, reading the second code word sequence data written in the second memory while applying a second interleave to the second code word sequence data, and recording alternately at a predetermined cycle the synchronization code, the code word sequence data applied with the first interleave, and the second code word sequence data applied with the second interleave.

56. The data recording method according to claim 55, wherein flags corresponding to the synchronization code, the first code word sequence data, and the second code word sequence data are set in the recording sequence of the recorded data, and a source of reading is switched based on these flags between a unit that generates the synchronization code, the first memory, and the second memory.

57. The data recording method according to claim 55, wherein the first memory and the second memory are areas disposed in the same buffer memory, and the first code word sequence data and second code word sequence data are written to respectively allocated areas in the buffer memory.

58. A method for recording data to a recording medium according to a format having alternating first data and second data, comprising:

error-correcting the first data to generate first code word sequence data;

error-correcting the second data to generate second code word sequence data;

generating synchronization codes;

dividing the first code word sequence data into a predetermined number of segments; and

applying a first interleave to the first code word sequence data segments to generate first recording-order arranged data segments,

applying a second interleave to the second code word sequence data to generate second recording-order arranged data, and

recording alternately the synchronization codes, the first recording-order arranged data, and the second recording-order arranged data in a predetermined cycle.

59. A method for recording data to a recording medium according to a format having alternating first data and second data, comprising:

applying error-correcting coding to the first data and writing first code word sequence data to a first memory;

applying error-correcting coding to the second data and writing second code word sequence data to a second

memory;

dividing the first code word sequence data into a predetermined number of code word sequence segments;

writing one segment of the first code word sequence data to a third memory;

generating synchronization codes; and

reading the first code word sequence data segments from the third memory while applying a first interleave to the first code word sequence data segments to generate first recording-order arranged data segments, reading the second code word sequence data from the second memory while applying a second interleave to the second code word sequence data segments to generate second recording-order arranged data, and recording alternately the synchronization codes, the first recording-order arranged data segment, and the second recording-order arranged data in a predetermined cycle.

60. The data recording method according to claim 59, wherein flags corresponding to the synchronization detection information, the first code word sequence data, and the second code word sequence data are set in the recording sequence of the recorded data, and a source of reading is switched based on these flags between a unit that generates the synchronization code, the second memory, and the third memory.

61. The data recording method according to claim 59, wherein the first memory and second memory are areas disposed in the same buffer memory, and the first code word sequence data and second code word sequence data are written to respectively allocated areas in the buffer memory.

62. A circuit for reproducing data from a recording

medium to which data is recorded in a format having a synchronization code, first recording-order arranged data, and second recording-order arranged data alternating in a predetermined cycle,

the first recording-order arranged data acquired by applying a first interleave to first encoded data, the first encoded data provided by applying error-correcting coding to the first data, and

the second recording-order arranged data acquired by applying a second interleave to second encoded data, the second encoded data provided by applying error-correcting coding to the second data,

the reproducing circuit comprising:

a separating unit that separates recorded data read from the recording medium to generate the synchronization code, the first recording-order arranged data, and the second recording-order arranged data;

a first code generator that generates first code word sequence data by applying a first interleave to the first recording-order arranged data;

a second code generator that generates second code word sequence data by applying a second interleave to the second recording-order arranged data;

a code word sequence error location generator for error-correcting the second code word sequence data to generate data error location information corresponding to the order of the second code word sequence data;

a recording-order arranged error location generator for applying a second interleave to the data error location information corresponding to the order of the second code word sequence data to generate data error location information in the order of the second recording-order arranged data;

a synchronization error extracting unit that extracts synchronization error information from the

synchronization code;

a data error location generator that generates first data error location information by combining in the recording sequence of the recorded data the synchronization error information and the data error location information in the order of the second recording-order arranged data;

a recording-order arranged erasure pointer generator that generates erasure pointers indicating erasure positions of first data, from the first data error location information, the pointers corresponding to the order of the first recording-order arranged data;

a code word sequence erasure pointer generator that applies a first deinterleave to the erasure pointers corresponding to the order of the first recording-order arranged data to generate erasure pointers in the order of the first code word sequence data; and

a correcting unit that applies error-correcting for erasure to the first code word sequence data using the erasure pointers corresponding to the order of the first code word sequence data.

63. The data reproducing circuit according to claim 62, wherein the recording-order arranged erasure pointer generator generates erasure pointers by determining from the first data error location information whether errors occur in the second recording-order arranged data or synchronization code continuously in the recording direction of the recorded data.

64. A circuit for reproducing data from a recording medium to which data is recorded in a format having a synchronization code, first recording-order arranged data, and second recording-order arranged data alternating in a predetermined cycle,

the first recording-order arranged data acquired

by applying a first interleave to first encoded data, the first encoded data provided by applying error-correcting coding to first data, and

the second recording-order arranged data acquired by applying a second interleave to second encoded data, the second encoded data provided by applying error-correcting coding to second data,

the reproducing circuit comprising:

a separating and deinterleaving unit that separates recorded data read from the recording medium, generates the synchronization code, the first recording-order arranged data, and the second recording-order arranged data, extracts synchronization error information from the synchronization code, applies a first deinterleave to the first recording-order arranged data to generate first code word sequence data, and applies a second deinterleave to the second recording-order arranged data to generates second code word sequence data;

error location generator that error-corrects the second code word sequence data to generate data error location information corresponding to the order of the second code word sequence data;

erasure pointer generator that generates erasure pointers corresponding to the order of the first recording-order arranged data, from the data error location information and synchronization error information, the erasure pointers denoting data erasure locations in the first data; and

correcting unit that applies error-correcting for erasure to the first code word sequence data using the erasure pointers while applying a first deinterleave to the erasure pointers.

65. A circuit for reproducing data from a recording medium to which data is recorded in a format having a

synchronization code, first recording-order arranged data, and second recording-order arranged data alternating in a predetermined cycle,

the first recording-order arranged data acquired by applying a first interleave to first encoded data, the first encoded data provided by applying error-correcting coding to first data, and

the second recording-order arranged data acquired by applying a second interleave to second encoded data, the second encoded data provided by applying error-correcting coding to second data,

the reproducing circuit comprising:

first to fifth memories;

a separating and deinterleaving unit that separates recorded data read from the recording medium to generate the synchronization code, the first recording-order arranged data, and the second recording-order arranged data, extracts synchronization error information from the synchronization code and writing it in the first memory, applies a first deinterleave to the first recording-order arranged data to generate first code word sequence data and write it to the second memory, and applies a second deinterleave to the second recording-order arranged data to generate second code word sequence data and write it to the third memory;

an error location generator that error-corrects the second code word sequence data and writes data error location information corresponding to the order of the second code word sequence data to the fourth memory;

a erasure pointer generator that generates erasure pointers denoting erasure locations in the first data and corresponding to the order of the first recording-order arranged data, from the data error location information and synchronization error information, and writing it to the fifth memory; and

a correcting unit that applies error-correcting for erasure to the first code word sequence data using the erasure pointers while applying a first deinterleave to the erasure pointers.

66. The data reproducing circuit according to claim 65, wherein the second memory and the third memory are areas in the same buffer memory, and the first code word sequence data and second code word sequence data are written to respectively allocated areas in the buffer memory.

67. The data reproducing circuit according to claim 65, wherein flags corresponding to the synchronization error information, the first recording-order arranged data, and the second recording-order arranged data are set in the order of the recorded data, and a destination of writing is switched based on these flags between the first memory, an area in the buffer memory for the first code word sequence data, and an area in the buffer memory for the second code word sequence data.

68. The data reproducing circuit according to claim 65, wherein the data error location information in the order of the second code word sequence data allocates one bit to one byte of the second code word sequence data, and manages error location information for one column of the second code word sequence data using m-bytes (where m is an integer) of data.

69. The data reproducing circuit according to claim 65, wherein according to a format of the synchronization error information, one byte is allocated to one synchronization detection information, and plural bytes of synchronization detection information are arranged in the

order of the recorded data.

70. The data reproducing circuit according to claim 65, wherein the first recording-order arranged erasure pointer contains plural bytes, each byte denotes erasure location information, and the bytes are arranged in the order of the first recording-order arranged data.

71. The data reproducing circuit according to claim 65, wherein the first memory, the fourth memory, and the fifth memory are allocated in areas of one small capacity memory.

72. The data reproducing circuit according to claim 71, wherein the small capacity memory has two areas for storing the synchronization error information, one area for storing the data error location information, and one area for storing the erasure pointers.

73. A circuit for reproducing data from a recording medium to which data is recorded in a format having a synchronization code, first recording-order arranged data, and second recording-order arranged data alternating in a regular cycle,

the first recording-order arranged data acquired by applying a first interleave to first encoded data, the first encoded data provided by applying error-correcting coding to first data, and

the second recording-order arranged data acquired by applying a second interleave to second encoded data, the second encoded data provided by applying error-correcting coding second data,

the reproducing circuit comprising:

a second recording-order arranged data generator that separates recorded data read from the recording medium

to generate the synchronization code, the first recording-order arranged data, and the second recording-order arranged data;

a data segment generator that divides the first recording-order arranged data into plural data segments, applying a first deinterleave to each data segment, and generating plural first code word sequence data segments;

a data segment assembling unit that assembles the plural first code word sequence data segments and generating first code word sequence data;

a second code word sequence data generator that applies a second deinterleave to the second recording-order arranged data to generate second code word sequence data;

a code word sequence error location generator that error-corrects the second code word sequence data to generate data error location information corresponding to the order of the second code word sequence data;

a recording-order arranged error location generator that applies a second interleave to the data error location information corresponding to the order of the second code word sequence data to generate data error location information corresponding to the order of the second recording-order arranged data;

a synchronization error information extracting unit for extracting synchronization error information from the synchronization code;

a combining unit that generates first data error location information by combining, in the recording sequence of the recorded data, the synchronization error information and the data error location information in the order of the second recording-order arranged data;

a first recording-order arranged erasure pointer generator that generates erasure pointers indicating erasure locations in the first data corresponding to the order of the first recording-order arranged data, from the

first data error location information;

a first code word sequence erasure pointer generator that applies a first deinterleave to the erasure pointers to generate erasure pointers corresponding to the order of the first code word sequence data; and

a correcting unit that applies error-correcting for erasure to the first code word sequence data using the erasure pointers corresponding to the order of the first code word sequence data.

74. The data reproducing circuit according to claim 73, wherein the first recording-order arranged erasure pointer generator determines, from the first data error location information, whether an error for the second recording-order arranged data or synchronization code occurs in the first data error location information, continuously in the recording direction of the recorded data, thus to generate the erasure pointer.

75. A circuit for reproducing data from a recording medium to which data is recorded in a format having a synchronization code, first recording-order arranged data, and second recording-order arranged data alternating in a regular cycle,

the first recording-order arranged data acquired by applying a first interleave to first encoded data, the first encoded data provided by applying error-correcting coding to first data, and

the second recording-order arranged data acquired by applying a second interleave to second encoded data, the second encoded data provided by applying error-correcting coding to second data,

the reproducing circuit comprising:

a separating and deinterleaving unit that separates recorded data read from the recording medium to

generate the synchronization code, the first recording-order arranged data, and the second recording-order arranged data, extracts synchronization error information from the synchronization code, divides the first recording-order arranged data into plural data segments, applies a first deinterleave to each data segment to generate plural first code word sequence data segments, and applies a second deinterleave to the second recording-order arranged data to generates second code word sequence data;

assembling unit that assembles the plural first code word sequence data segments to generate first code word sequence data;

error location generator that error-corrects the second code word sequence data to generate data error location information corresponding to the order of the second code word sequence data;

erasure pointer generator that generates erasure pointers denoting erasure locations of the first recording-order arranged data from the data error location information and synchronization error information, the erasure pointers arranged in the order of the first recording-order arranged data; and

correcting unit that applies error-correcting for erasure to the first code word sequence data using the erasure pointers while deinterleaving the erasure pointers.

76. A circuit for reproducing data from a recording medium to which data is recorded in a format having a synchronization code, first recording-order arranged data, and second recording-order arranged data alternating in a regular cycle,

the first recording-order arranged data acquired by applying a first interleave to first encoded data, the first encoded data provided by applying error-correcting coding to first data, and

the second recording-order arranged data acquired by applying a second interleave to second encoded data, the second encoded data provided by applying error-correcting coding to second data,

the reproducing circuit comprising:

first to fifth memories;

an extracting and deinterleaving unit that separates recorded data read from the recording medium to generate the synchronization code, the first recording-order arranged data, and the second recording-order arranged data, extracts synchronization error information from the synchronization code to write it to the first memory, divides the first recording-order arranged data into plural data segments, applies a first deinterleave to each data segment to generate plural first code word sequence data segments and write them to the second memory, and applies a second deinterleave to the second recording-order arranged data to generate second code word sequence data to write it to the third memory;

a data assembling unit that sequentially writes the first code word sequence data segments from the second memory to the fourth memory to generate first code word sequence data;

an error location generator that error-corrects the second code word sequence data to write data error location information corresponding to the order of the second code word sequence data to the fifth memory;

a erasure pointer generator that generates erasure pointers denoting erasure position of the first data from the data error location information in the order of the second code word sequence data and synchronization error information and writes the erasure pointers to the sixth memory, the erasure pointers arranged in the order of the first recording-order arranged data; and

a correcting unit that applies error-correcting

for erasure to the first code word sequence data using the erasure pointers while applying a first deinterleave to the erasure pointers.

77. The data reproducing circuit according to claim 76, wherein the capacity of the second memory is smaller than the size of the first recording-order arranged data.

78. The data reproducing circuit according to claim 76, wherein the third memory and the fourth memory are areas in the same buffer memory, and the first code word sequence data and the second code word sequence data are written to respectively allocated areas in the buffer memory.

79. The data reproducing circuit according to claim 76, wherein flags corresponding to the synchronization detection information, the first recording-order arranged data, and the second recording-order arranged data are set in the order of the recorded data, and a destination of writing is switched based on these flags between the first memory, the second memory, and an area in the buffer memory for the second code word sequence data.

80. The data reproducing circuit according to claim 76, wherein the data error location information in the order of the second code word sequence data allocates one bit to one byte of the second code word sequence data, and manages error location information for one column of second code word sequence data using m-bytes (where m is an integer) of data.

81. The data reproducing circuit according to claim 76, wherein according to a format of the synchronization error information, one byte is allocated to one

synchronization detection information, and plural bytes of synchronization detection information are arranged in the order of the recorded data.

82. The data reproducing circuit according to claim 76, wherein the first recording-order arranged erasure pointer contains plural bytes, each byte denotes erasure location information, and the bytes are arranged in the order of the first recording-order arranged data.

83. The data reproducing circuit according to claim 76, wherein the first memory, the fifth memory, and the sixth memory are allocated in areas of one small capacity memory.

84. The data reproducing circuit according to claim 76, wherein the small capacity memory has two areas for storing the synchronization error information, one area for storing the second data error location information, and one area for storing the first recording-order arranged erasure pointers.

85. A circuit for recording data to a recording medium according to a format having alternating first data and second data, comprising:

a first code generator that error-corrects the first data to generate first code word sequence data;

a second code generator that error-corrects the second data to generate second code word sequence data;

a synchronization code generator that generates synchronization codes; and

a recording data generator that applies a first interleave to the first code word sequence data to generate first recording-order arranged data, applies a second interleave to the second code word sequence data to

generate second recording-order arranged data, and records alternately the synchronization codes, the first recording-order arranged data, and the second recording-order arranged data in a predetermined cycle.

86. A circuit for recording data to a recording medium according to a format having alternating first data and second data, comprising:

a first memory and a second memory;

a first code generator that error-corrects the first data to generate and write first code word sequence data to the first memory;

a second code generator that error-corrects the second data to generate and write second code word sequence data to the second memory;

a synchronization code generator that generates synchronization codes; and

a recording data generator that reads, while applying a first interleave, the first code word sequence data, reads, while applying a second interleave, the second code word sequence data, and records alternately to the recording medium at a predetermined cycle the synchronization code, the interleaved first code word sequence data a, and the interleaved second code word sequence data.

87. The data recording circuit according to claim 86, wherein flags corresponding to the synchronization code, the code word sequence data for the first data, and the code word sequence data for the second data are set in the recording-order arranged of the recorded data, and a source of reading is switched based on these flags between the synchronization code generator, the first memory, and the second memory.

88. The data recording circuit according to claim 86, wherein the first memory and the second memory are disposed in an area of the same buffer memory, and the first code word sequence data and second code word sequence data are written to respectively allocated areas in the buffer memory.

89. A circuit for recording data to a recording medium according to a format having alternating first data and second data, comprising:

a first code generator that error-corrects the first data to generate first code word sequence data;

a second code generator that error-corrects the second data to generate second code word sequence data;

a dividing unit that divides the first code word sequence data into a predetermined number of code word sequence data segments;

a synchronization code generator that generates synchronization codes;

a recording data segment generator that applies a first interleave to the code word sequence data segments to generate first recording data segments, applies a second interleave to the second code word sequence data to generate second recording-order arranged data, and arranges alternately the synchronization codes, the first recording data segments, and the second recording-order arranged data in a predetermined cycle to generate a recording data segment; and

an evaluating unit that determines whether a recording data segment has been generated using all first recording data segments.

90. A circuit for recording data to a recording medium according to a format having alternating first data and second data, comprising:

first memory to third memory;

a first code generator that applies error-correcting coding to the first data to generate and write first code word sequence data to the first memory;

a second code generator that applies error-correcting coding to the second data to generate and writ second code word sequence data to the second memory;

a dividing unit that divides the first code word sequence data into a predetermined number of code word sequence data segments;

a memory writing unit that writes the code word sequence data segment to the third memory;

a synchronization code generator that generates synchronization code;

a recording segment generator that reads the first code word sequence data segment from the third memory, applies a first interleave to the segment to generate first recording data segment, reads the second code word sequence data from the second memory and applies a second interleave to the read data to generate second recording-order arranged data, and arranges alternately the synchronization code, the first recording-order arranged data segment, and the second recording-order arranged data in a predetermined cycle to generate recording data segment; and

evaluating unit that determines whether the recording segments has been generated using all divided first recording data segments.

91. The data recording circuit according to claim 90, wherein flags corresponding to the synchronization code, the first code word sequence data, and the second code word sequence data are set in the recording-order arranged of the recorded data, and a source of reading is switched based on these flags between the synchronization code generator, the third memory, and the second memory.

92. The data recording circuit according to claim 90, wherein the first memory and second memory are disposed in the same buffer memory, and the first code word sequence data and the second code word sequence data are written to respectively allocated areas in the buffer memory.

93. A data reproducing apparatus comprising:

a unit that reads data from a recording medium to which data is recorded in a predetermined data format; and

the data reproducing circuit according to claim 62 that error-corrects the read data to generate desired data.

94. A data reproducing apparatus comprising:

a unit that reads data from a recording medium to which data is recorded in a predetermined data format; and

the data reproducing circuit according to claim 64 that error-corrects the read data to generate desired data.

95. A data reproducing apparatus comprising:

a unit that reads data from a recording medium to which data is recorded in a predetermined data format; and

the data reproducing circuit according to claim 65 that error-corrects the read data to generate desired data.

96. A data reproducing apparatus comprising:

a unit that reads data from a recording medium to which data is recorded in a predetermined data format; and

the data reproducing circuit according to claim 73 that error-corrects the read data to generate desired data.

97. A data reproducing apparatus comprising:

a unit that reads data from a recording medium to which data is recorded in a predetermined data format; and

the data reproducing circuit according to claim 75 that error-corrects the read data to generate desired data.

98. A data reproducing apparatus comprising:

a unit that reads data from a recording medium to which data is recorded in a predetermined data format; and

the data reproducing circuit according to claim 76 that error-corrects the read data to generate desired data.

99. A data recording apparatus comprising:

a signal processing circuit that generates data to be recorded;

a data recording circuit according to claim 85 that receives the data to be recorded and generates recording data in a predetermined data format; and

a unit that records the recording data of the predetermined data format to a recording medium.

100. A data recording apparatus comprising:

a signal processing circuit that generates data to be recorded;

a data recording circuit according to claim 86 that receives the data to be recorded and generates recording data in a predetermined data format; and

a unit that records the recording data of the predetermined data format to a recording medium.

101. A data recording apparatus comprising:

a signal processing circuit that generates data to be recorded;

a data recording circuit according to claim 89 that receives the data to be recorded and generates recording data in a predetermined data format; and

a unit that records the recording data of the predetermined data format to a recording medium.

102. A data recording apparatus comprising:

a signal processing circuit that generates data to be recorded;

a data recording circuit according to claim 90 that receives the data to be recorded and generates recording data in a predetermined data format; and

a unit that records the recording data of the predetermined data format to a recording medium.